

P-23

NASA CASE NO. MFS-28855-1

PRINT FIG. #1

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(NASA-Case-MFS-28855-1)
MULTI-SPEED MULTI-PHASE RESOLVER
CONVERTER Patent Application
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MULTI-SPEED MULTI-PHASE RESOLVER CONVERTER

This invention relates to a multi-phase converter circuit for use with an angular resolver system. The invention provides an improved and low cost way of deriving, for example, 3-phase excitation signals to drive a 24-speed
5 brushless motor in synchronism with signals provided by a single speed 2-phase analog resolver.

Referring now to **Figure 1**, reference 10 designates a preferred embodiment of the converter system. Analog signals provided attendant to rotation of a shaft 13 of an analog
10 resolver 12 are supplied to a sixteen bit resolver-to-digital converter from terminals 18, 20, 22, 24. In the exemplary form of the invention, the analog resolver 12 is a single speed 2-phase unit producing in parallel format on a plurality of output lines L1 digital numbers of increasing value as the
15 resolver shaft 13 is rotated. These digital numbers are fed simultaneously to the address terminals of a plurality of addressable digital memory systems 28, 30, 32, each system having stored therein at sequential addresses sequential values of a wavetrain of sinusoids of given number common to
20 all of the memory systems. The sinusoidal wavetrains and the values corresponding thereto are displaced in phase with respect to the wavetrains associated with each of the remaining memory systems. Sequential values of the stored sinusoidal wavetrains are outputted at memory system output

terminals on lines L2, L3, L4 to associated sixteen bit digital-to-analog converters 34, 36, 38, which convert the wavetrain values received into analog form at system output terminals 40, 42, 44. To produce 3-phase output to excite a 24-speed (48-pole) motor the sequentially stored values in each of the memory systems 28, 30, 32 represent incremental values along a sinusoidal wavetrain having 24 sinusoids each. A modification of the memory systems and the phase displacement between the stored wavetrains may be carried out to provide for proper excitation of a multi-speed 2-phase motor.

The prior art customarily employs a relatively expensive multi-speed analog type angular resolver in conjunction with a resolver converter circuit to provide high speed value motor excitation. The present invention allows use of a low speed value analogue angular resolver to produce such excitation with a marked reduction in cost, as well as weight. It is anticipated that the reduced size, weight, and cost of the present system will be of particular value in space applications.

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PATENT APPLICATION

MULTI-SPEED MULTI-PHASE RESOLVER CONVERTER

ORIGIN OF THE INVENTION

This invention was made by employees of the United States Government and may be manufactured and used by or for the government for governmental purposes without the payment of
5 any royalties.

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The field of the invention is the electrical motor art, and in particular means for supplying multi-phase excitation
10 to poly-phase brushless motors.

(2) DESCRIPTION OF RELATED ART

This invention originated from a need to develop an inexpensive brushless direct current motor controller for a space station experiment pointing system. A brushless D.C.
15 motor can be commutated using several different methods. The first method, six-step commutation, causes an undesirable torque ripple in the pointing system, while the second method, sinusoidal commutation, does not. Because the torque ripple would cause an undesirable jitter in the pointing control,
20 sinusoidal commutation is preferred. Problems arise when the number of poles becomes excessive, as for example with a 48 pole, 3-phase brushless D.C. motor. The back electromotive force (EMF) of a permanent magnet brushless motor will cycle sinusoidally, and the number of cycles is equal to one-half

the number of poles per mechanical revolution of the motor. To minimize the torque ripple, the current applied to the motor must be in phase with the motor back EMF. (For a complete description of the four quadrant control of a brushless 3-phase motor , see U.S. Patent No. 4,644,234.) As shown in the brushless commutation literature, if the current and back EMF are in phase, then the following relationship for torque is valid:

$$T=[\sin^2(\theta)+\sin^2(\theta+2\pi/3)+\sin^2(\theta+4\pi/3)]\cdot K_m\cdot I=1.5\cdot K_m\cdot I$$

10 where T = total motor torque;

K_m = torque constant of the motor;

I = motor current; and

θ = angle of rotor magnets with respect to the stator windings

15 To generate the sinusoidally varying current, an angular position sensor which has the same frequency and is in phase with the motor back EMF has traditionally been required. The previous method for converting sinusoidal commutations of multi-pole D.C. brushless motors was to employ a multi-speed resolver. For the motor selected, a 48-pole (24-speed) unit, a 3-phase resolver would be required to perform the commutation. This type of resolver is commercially available, but not as an off-the-shelf item. To custom manufacture one would be prohibitively expensive and time consuming, and would have undesirable size and weight factors for space applications. There is a need for an inexpensive solution to this problem. This invention is directed to a solution of

these and related problems.

SUMMARY OF THE INVENTION

A multi-phase digital converter circuit for use with an angular resolver system is disclosed, the angular resolver system providing in parallel format on a plurality of resolver system output terminals a digital signal indicative of the angular position of an angular position sensor. In one form of the invention, the angular resolver system includes a single speed 2-phase analog resolver having its analog output connected to drive a resolver-to-digital converter circuit. The resolver-to-digital converter circuit in turn produces in parallel format on a plurality of output terminals the above mentioned digital signals. The digital multi-phase converter circuit includes a plurality of addressable digital memory systems, each system having address and data terminals and having stored therein at sequential addresses sequential values of a wave train of sinusoids of given number common to all of the memory systems. The wave train values in each memory system represent a sinusoidal wave train; however, the sinusoidal wave trains and the values corresponding thereto are displaced in phase with respect to the wave trains associated with each of the remaining memory systems. Each memory system is connected at its address terminals to receive simultaneously the digital signals produced by the angular resolver system. Simultaneous sequential addressing of the memory systems will cause sequential values of the stored

sinusoidal wave trains to be outputted at memory system output terminals. A digital-to-analog converter is connected to the output of each of the memory system output terminals and converts the wave train values received into analog form to be
5 presented at converter circuit output terminals.

In one form of the invention, as applied to producing 3-phase output to excite a 24-speed (48-pole) motor, the sequentially stored values in each of the memory systems represent incremental values along a sinusoidal wave train
10 having 24 sinusoids each. The number of memory systems is 3, and the 3 sets of wave trains are displaced from each other by 120 degrees. A modification of the memory systems and the phase displacement between the stored wave trains may be carried out to provide for proper excitation of a multi-speed
15 2-phase motor.

Alternative input systems for providing digital position-indicating signals on the address lines of the memory systems include an absolute optical encoder for producing direct digital representations of the angular position of its
20 associated shaft, and a multi-pulse incremental encoder for producing sequential pulses as the encoder rotation increases, the pulses being conveyed to a counter to be converted to a digital representation at the counter output.

Other advantages and features of invention will become
25 apparent upon making reference to the specifications, claims and drawings to follow.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a block diagram of a multi-phase converter circuit designed to produce 3-phase output from digital signals provided by an analog angular resolver feeding a
5 resolver-to-digital converter.

Figure 2A shows the relationship between one resolver phase and a 28 cycle sinusoidal wave form generated by conversion of the resolver output signal.

Figure 2B shows the relationship of motor back EMF and
10 one phase of motor current when the resolver of **Figure 1** is connected to drive a motor, and the resolver is properly oriented with respect to the motor shaft.

Figures 3A - 3D show a schematic circuit performing the functions indicated in **Figure 1**.

15 **Figure 4** shows the use of an absolute encoder to supply digital data to the converter shown in **Figure 1**.

Figure 5 shows the use of an incremental encoder and a digital counter to provide digital data to the circuit shown in **Figure 1**.

20 DESCRIPTION OF THE PREFERRED EMBODIMENTS

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail a preferred embodiment of the invention with the understanding that the present disclosure
25 is to be considered as an exemplification of the principles of the invention, and is not intended to limit the broad aspect

of the invention to the embodiments illustrated.

The present invention is mainly concerned with a multi-phase converter for producing from low-speed angular resolvers multi-phase excitation signals for driving multi-phase
5 brushless motors of speed value higher than that of the resolver system. A multi-phase converter circuit is designed for use with an angular resolver system, the angular resolver system providing in parallel format on a plurality of resolver system output terminals a digital signal indicative of the
10 angular position of an angular resolver. In the preferred form of the invention, the angular resolver system includes a single speed (speed value 1) 2-phase analog resolver having its output connected to drive a resolver-to-digital converter. The digital converter in turn produces in parallel format on
15 a plurality of output terminals the above mentioned digital signals. The multi-phase converter circuit includes a plurality of addressable digital memory systems, each system having address and data terminals and having stored therein at sequential addresses sequential values of a wave train of
20 sinusoids of given number common to all of the memory systems. The wave train values in each of the memory systems represent a sinusoidal wave train; however, the sinusoidal wave trains and the values corresponding thereto are displaced in phase with respect to the wave trains associated with each of the
25 remaining memory systems. The memory systems are configured as table look-up systems. Each memory system is connected at its

address terminals to receive simultaneously digital signals produced by the angular resolver system, in the preferred embodiment from an analog resolver-to-digital converter system. Simultaneous sequential addressing of the memory
5 systems will cause the values of these stored sinusoidal wave trains to be outputted at system memory output terminals in parallel format. A digital-to-analog converter is connected to the output of each of the memory systems and converts the wave train values received into analog form to be presented at
10 system output terminals.

In more detail, **Figure 1** shows a block diagram for a single speed 2-phase to 24 speed 3-phase resolver converter. An analog resolver 12 is excited by a sinusoidal signal, $K_E \cdot \sin(\omega t)$, applied to terminals 14, 16, resulting in the
15 conventional modulated sine and cosine analog outputs $K_R \cdot \sin(\omega t) \cdot \sin(\theta)$ and $K_R \cdot \sin(\omega t) \cdot \cos(\theta)$ at terminals 18, 20 and 22, 24 respectively, where K_R is a constant, ω is the excitation frequency, and θ is the angle of resolver shaft 13. Typical excitation values are 5 volts at 5 kilohertz. These outputs
20 are the inputs to a resolver-to-digital (R/D) converter 26. The R/D converter 26 takes the signals and produces on lines L1 a 16-bit digital word corresponding to the angle of the resolver shaft 13.

Lines L1 communicate these words to a digital multiphase
25 converter circuit 10. The 16-bit word is used to address each of three 64K programmable memory IC (EPROM) systems 28, 30,

32.

analog resolver 12

The particular ~~R/D converter 26~~ is a model 25R77G-71A made by American Electronics, Inc. of Culver City, California. Zero rotation of the resolver shaft 13 from a fiducial point results in a numerical output of 0000(H) on lines L1. Successive incremental rotation of the shaft 13 causes the output numbers to monotonically increase to a final terminal value of FFFF(H) at the completion of one revolution.

The first EPROM system 28 contains the digitized amplitudes of 24 sinusoidal waves in 64K increments. The second EPROM system 30 has the 24 sinusoidal values shifted $2\pi/3$ radians (120°), and the final EPROM system 32 contains the sine wave data shifted $4\pi/3$ radians (240°). The data stored in each EPROM system 28, 30, 32, is thus in the form of 64K 16-bit words, resulting in sinusoidal information which has a peak-to-peak accuracy of 16-bits and a 16-bit accuracy over 360 mechanical degrees i.e. 24 sinusoidal waves.

To avoid the necessity for employing a sign bit to accommodate negative values of the stored sinusoidal wave forms, and thereby to secure maximum utilization of memory capacity, the sequential values of the sinusoidal wave forms stored digitally in the EPROM systems 28, 30, 32 are stored in the form $1+\sin(24\cdot\theta+\Phi)$, where Φ is the phase angle associated with each memory unit, eg. $2\pi/3$, $4\pi/3$.

Each of these EPROM systems 28, 30, 32 feeds via lines L2, L3, L4 respectively associated 16-bit digital-to-analog

2/8/8
DCA
2/8/8

converters 34, 36, 38 (DAC) which convert the signal values stored in the EPROM systems 28, 30, 32 to analog values. The digital-to-analog converters 34, 36, 38 are type MM3292 bipolar units made by ~~Micro-Netzwerke~~ ^{Micro-Netzwerke} of Worcester, Massachusetts. Their biasing is arranged so that in response to an input number 0000 an analog output voltage of +10 volts is produced, in response to a digital input FFFF(H) an analog voltage of -10 is produced, and a half-range value corresponding the axis crossings of an unbiased sinusoidal wave train, namely an input number 7FFF gives rise to 0 volts at the output. This generates the 3-phase sinusoidal signals appearing at terminals 40, 42, and 44, each containing 24 cycles for one revolution of the resolver shaft 13.

Figure 2A shows the demodulated output of one resolver phase (curve W4) in synchronism with the generated 24 sinusoid wave train (curve W1). The signals appearing at terminals 40, 42, 44 serve to provide properly phased sinusoidal excitation for a 48-pole brushless D.C. motor through appropriate drivers (not shown). These signals are in synchronism with the sine and cosine waveforms of the single speed resolver 12, thus electronically producing the desired multiple speed resolver outputs from a single speed device.

Once the above described electronic system is set up, the resolver 12 can then be mechanically coupled to the shaft of the driven motor (not shown). By monitoring, for example, output terminal 40 and one phase of the motor, the resolver

2/8/44
DCA
EJA
2/9/44

can be mechanically adjusted so that the resolver signals (curve W2 in **Figure 2B**) are in phase with the motor back EMF (curve W3), thereby aligning the 3-phase sinusoidal signals with the 3-phase motor back EMF to provide excitation giving
5 rise to low torque ripple.

Figures 3A - 3D show a schematic diagram of a circuit for accomplishing the previously stated objectives. The functioning of this circuit will be evident to those of ordinary skill in the art. Resolver field excitation is
10 provided by a sinewave generator U4 having its output passed through driver U5 and a final driver U7. Reference sinusoidal excitation is derived from driver U5 and driver U6. The two resolver outputs are delivered to terminals 4 and 7 of a resolver-to-digital-converter integrated circuit U3,
15 preferably type AD2S80 made by Analog Devices, Inc. of Norwood, Massachusetts. Terminals 9-24 feed the address line groups previously designated as L1, and this address line group feeds in parallel the address terminals of memory elements M1, M2, M3, M4, M5, M6. Each of the memory elements
20 M1, M2, M3, M4, M5, M6 is a 64K i.e. 10000(H) memory element having storage capacity for 8-bit words. The memory elements M1-M6 are wired to provide high-byte/low-byte outputs. Thus, the paired arrangement consisting of memory elements M1 and M2 have the eight bits representing the most significant bits
25 (high bits) of each word stored in element M2, and the corresponding least significant bits stored in element M1.

Similar considerations apply to the storage of waveform information in M3, M4, M5 and M6. The eight data output lines of element M2 extending from pins 11 to 19 are fed to the most significant bit pins 1-8 of a digital-to-analog converter U11, and the data lines from terminals 11 to 19 of element M1 are connected to the lower bit value terminals of converter U11. Collectively, these two groups of 8 lines correspond to line L2 of **Figure 1**. Digital-to-analog converters U12 and U13 are similarly connected to the memory element pairs M3, M4 and M5, M6 to produce the desired 3-phase sinusoidal excitation at output terminals 40, 42, 44.

The single speed 2-phase to 24-speed 3-phase converter described above may easily be modified for use with 2-phase motors by eliminating one EPROM block and its associated digital-to-analog converter and by shifting the sinusoidal waveform data stored in memory units M3, M4 by $\pi/2$ (90°) from the waveform data in memory elements M1, M2.

The previous discussion has centered on the use of an analog type angular resolver producing modulated analog output signals. Other types of angular resolver systems may be employed. Thus, for example, as shown in **Figure 4**, an absolute encoder 43 such as an absolute optical encoder driven by a shaft 45 may be used to place digital values on lines L1' to provide digital inputs to the memory systems 28, 30, 32 of **Figure 1**. Alternatively, an incremental encoder unit 46 driven by a shaft 48 and producing an output pulse for each given

increment of rotation may be used to drive a counter 50, the count appearing on output lines L1". Because of the limited range of values available from either of the foregoing encoders 42, 46, a corresponding reduction in the number of output lines L1, L1' is shown. This in turn will allow a reduction in the necessary capacity of the memory systems 28, 30, 32 and a corresponding reduction in the number of lines in groups L2, L3, L4. The previously described versions employing an analog resolver-to-digital converter, an absolute encoder system, and an incremental encoder system, are all to be construed as being "angular resolver systems" in the sense of the claims. Moreover, the angular resolver 12, the absolute encoder 43, and the incremental encoder unit 46 are all to be construed as the being "angular position sensors".

While the invention has been described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the inventions not be limited to a particular embodiment disclosed as the best mode contemplated for carrying out the invention, but that the invention will include all embodiments falling within the scope of the appended claims. In particular,

although attention is focused solely on the use of single speed angular resolvers, it is clear that resolvers of higher speed value may have their outputs converted to still higher speed values by the multi-sine wavetrain storage method
5 outlined hereinabove.

ABSTRACT OF THE DISCLOSURE

A multiphase converter circuit generates a plurality of sinusoidal outputs of displaced phase and given speed value from the output of an angular resolver system attachable to a motor excited by these multi-phase outputs, the resolver system having a lower speed value than that of the motor. The angular resolver system provides in parallel format sequential digital numbers indicative of the amount of rotation of the shaft of an angular position sensor associated with the angular resolver system. These numbers are used to excite simultaneously identical addresses of a plurality of addressable memory systems, each memory system having stored therein at sequential addresses sequential values of a sinusoidal wavetrain of a given number of sinusoids. The stored wavetrain values represent sinusoids displaced from each other in phase according to the number of output phases desired. A digital-to-analog converter associated with each memory system converts each accessed word to a corresponding analog value to generate attendant to rotation of the angular resolver a sinusoidal wave of proper phase at each of the plurality of outputs. By properly orienting the angular resolver system with respect to the rotor of the motor, essentially ripple-free torque is supplied to the rotor. The angular resolver system may employ an analog resolver feeding an integrated circuit resolver-to-digital converter to produce the requisite digital values serving as addresses. Alternative

versions employing incremental or absolute encoders are also described.

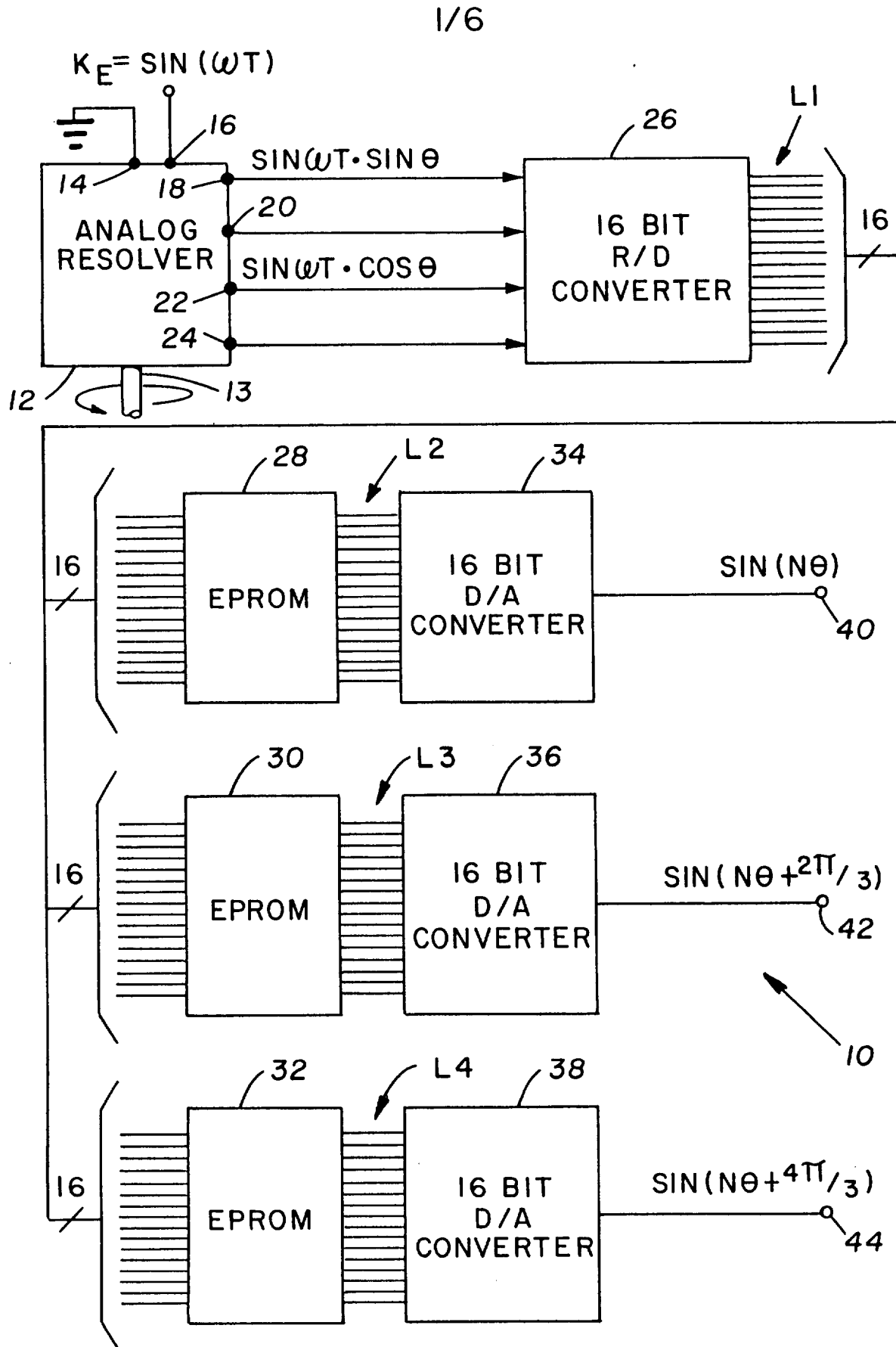


FIG. 1.

2/6

FIG. 2A.

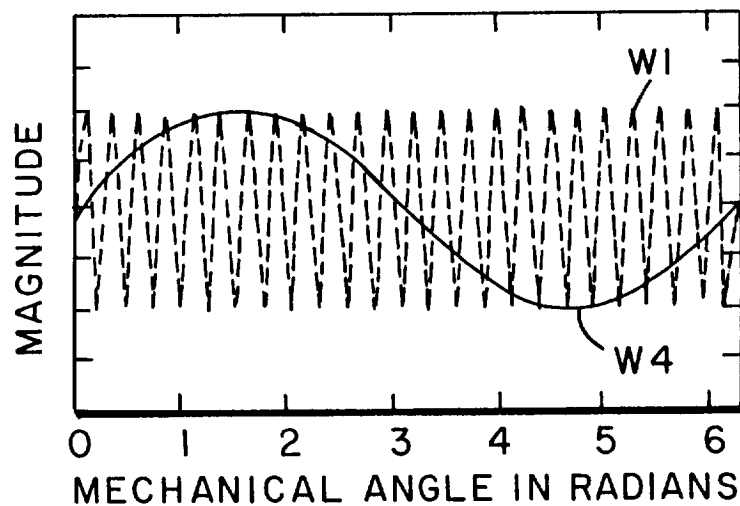


FIG. 2B.

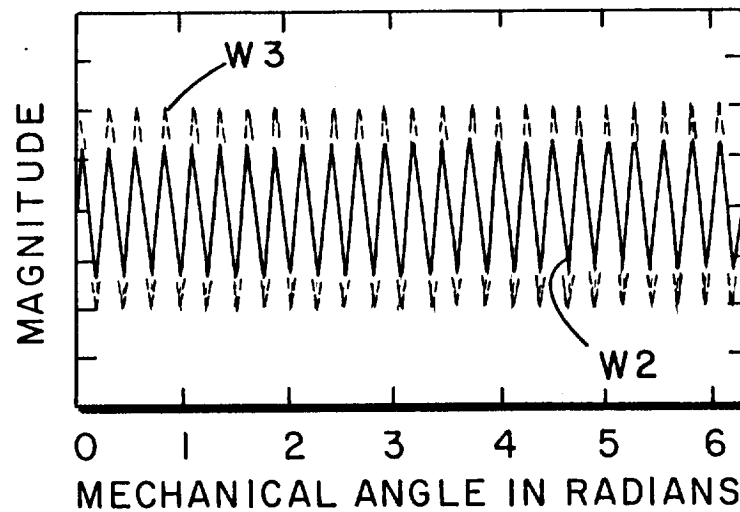


FIG. 4.

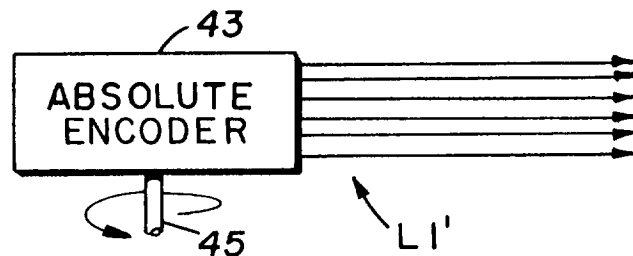
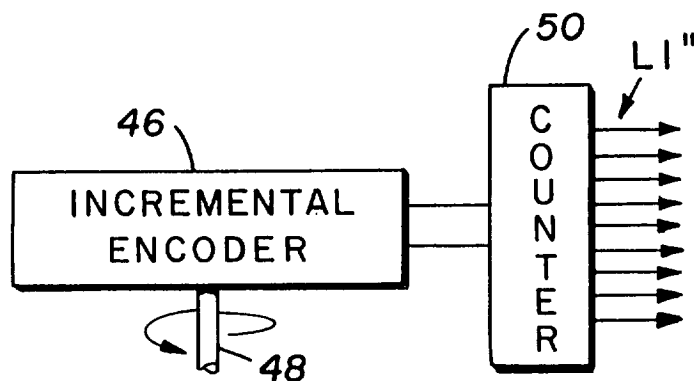


FIG. 5.



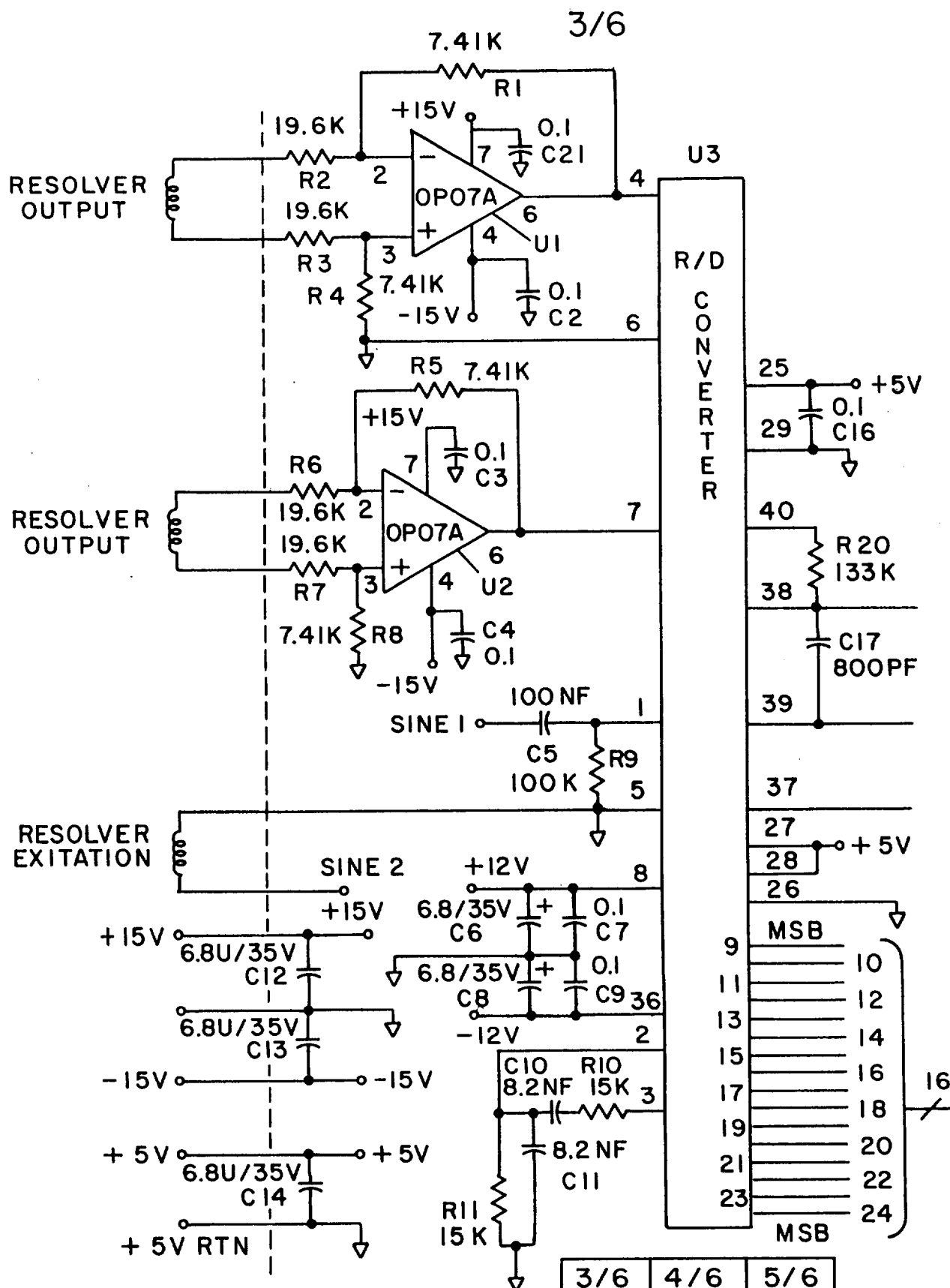
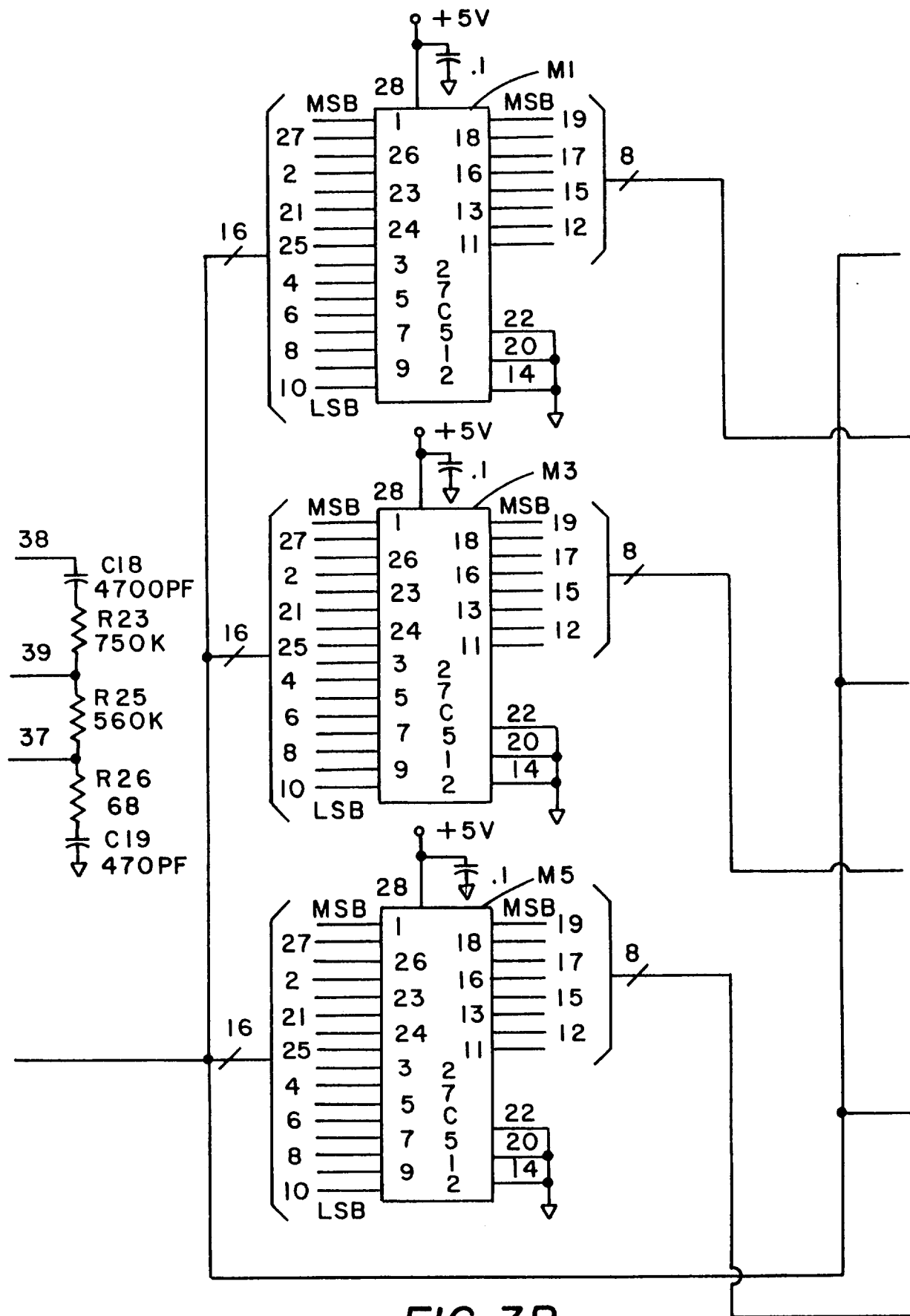


FIG. 3A.

3/6 FIG. 3A.	4/6 FIG. 3B.	5/6 FIG. 3C.
6/6 FIG. 3D.	SHEET PLAN	

4/6



5/6

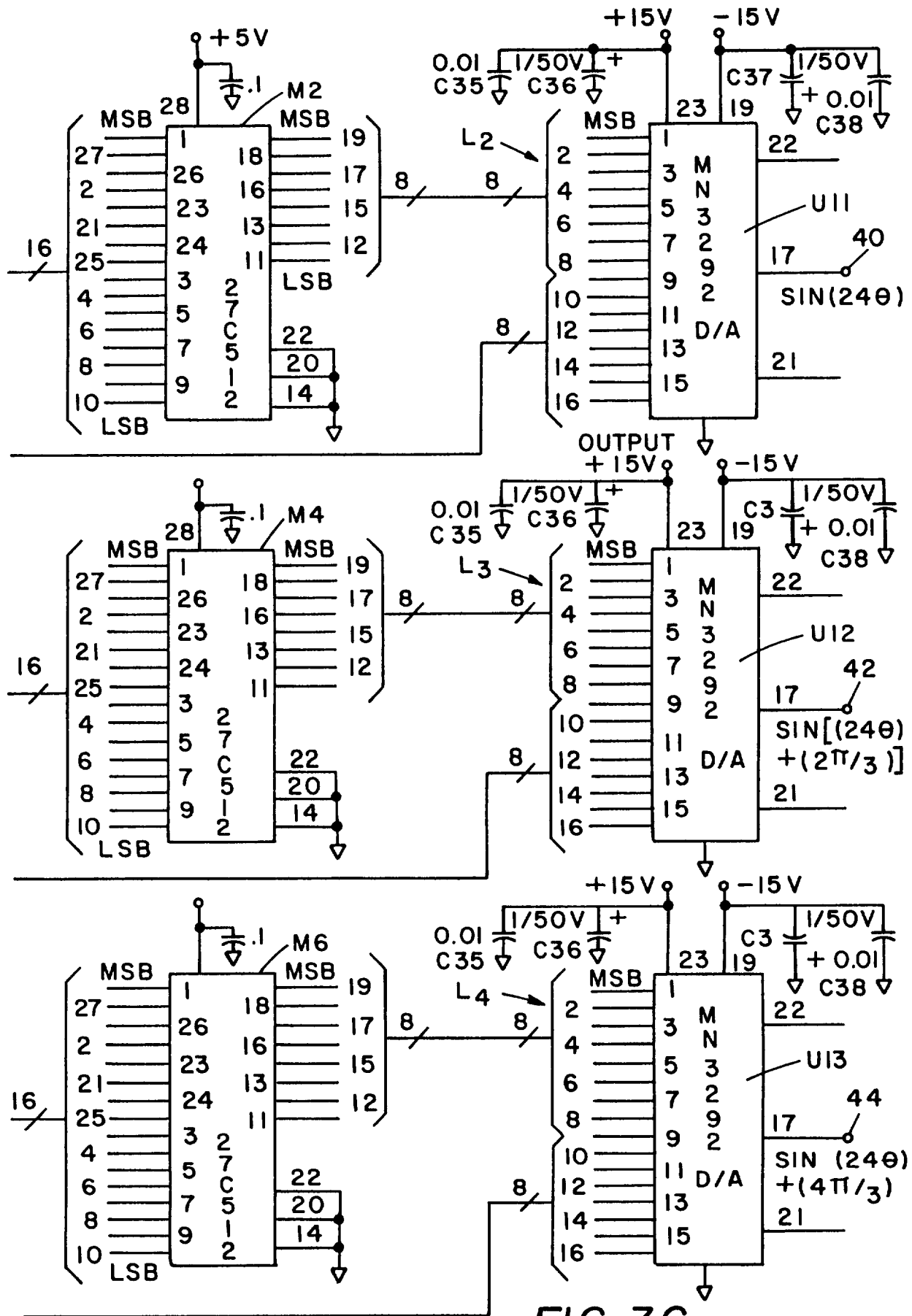


FIG 3C

